Current Trends in Technology and Science
www.ctts.in, ISSN: 2279-0535, March-2021, Volume: X, Issue: II

Enhancement Performance Static Random Access Memory Cell Using Switching Concept

Amrit Lal Kushwaha, Dharmendra Kumar Singh
Department of Digital Communication
Swami Vivekanand College of Science & Technology, Bhopal
amritlalkushwaha73@gmail.com, dharmendra.svcst@gmail.com

ABSTRACT- Enhancement performance static random access memory cell using a switching concept. This field research paper investigates the plan and examination of Static Random-Access recollections (SRAMs) that enhance postponement and power. CMOS SRAM cell eats up extraordinarily less power and has less scrutinise and create time. Higher cell proportions will diminish the peruse and compose time and improve soundness. PMOS semiconductor device with fewer dimensions reduces power consumption. During this paper, 6T SRAM cell is implemented with reduced power, and performance is nice according to read and write time, delay and power consumption. It's been seen regularly that expanded memory ability will build the cycle line parasitic capacitance that progressively hinders voltage detecting. To keep away from this disadvantage, utilise streamlined scaling methods, and the sky is the limit from there, improve the execution of the look. Memories are a core neighbourhood of most electronic systems. Performance in terms of speed and power dissipation is the main concern in today's memory technology. Read stability is one of the foremost important factors for designing an efficient SRAM cell. This exploration presents inside and out comprehension of the 6T-SRAM cell's usefulness and relative execution study of the bit-cell under three different technologies. Measures are taken to mitigate the effect of a drastic reduction in the read-static-noise margin at 16nm CMOS technology by implementing the 9TSRAM structure. To plan an SRAM cell, inside the current exploration, read and hold security are mulled over. At that point, static commotion edges are assessed for hold and peruse activities by fastidiously choosing the cell-boundaries. The cell proportion has profoundly affected the operation of the memory cell. Temperature dependence is additionally analysed for 6T and 9T cell at 16nm technology. During this paper, SRAM cells supported 6T, 9Tand 8T configurations are compared on the idea of performance for reading and write operations during this paper, totally extraordinary static arbitrary access memory is planned so on fulfil low power, high-performance circuit and also the extensive survey on options of assorted static random-access memory (SRAM) designs were reported. Proposed static random-access memory supported switching concept PSBSC is designing a coffee power SRAM cell structure with optimum write access power.

Keywords: Static Random-Access Memory, Delay, Power, Six Transistors, Write Delay, Read Delay, Power Consumption, Read Stability.

I. INTRODUCTION

Random-access memory (RAM) is a form of pc data storage that stores frequently used program instructions to extend the final speed. A random-access device permits knowledge to be read or written in nearly the same quantity of your time, irrespective of the physical location of information within the memory. In contrast, with different direct-access data storage media comparable to hard disks, CD-RWs, DVD-RWs and also the older drum memory, the time needed to read and write knowledge things varies considerably depending on their physical locations on the recording medium because of mechanical limitations such as media rotation speeds and arm movement Static Random-Access memories (SRAM) is scan/write memory devices which will read data from or write data to any of its memory addresses. The requirement for low power integrated circuits is well known due to their extensive use within portable electronic equipment. On-chip SRAMs (Static Random-Access Memory) confirm the power dissipation of SoCs (System on Chips) additionally to its speed of operation. Therefore, it is important to own energy economical SRAMs. The use of SRAM is expected to extend in future for each portable and high-performance microchip. SRAM plays a crucial role in modern microchip system, portable devices like PDA, cellular phones, and transportable multimedia system devices. SRAM primarily based cache memories are ordinarily used to achieve a higher speed microchip.

The device's scaling brings many challenges like power dissipation, sub-threshold run, reverse diode run, and stability [1]. These days, the low threshold voltage and ultra-thin gate chemical compound analysis are in the progressive stage, thanks to reducing the threshold voltage and the gate oxide thickness. The phenomena like intrinsic parameter fluctuation, random dopant fluctuation, oxides thickness fluctuation, and line edge roughness degrade SRAM cells' stability. Giant scale integration and fabrication process have increased the density of devices by decreasing the physical device dimensions. Performance in low power dissipation and high-speed operation is the most important computer circuit in deep submicron and nanoscale technologies. Designing a high-performance VLSI chip is becoming a

necessity for mobile communication and computing devices. Advances in battery technology haven't taken place as quick as advances within electronic devices and systems. So, designing electronic systems with high-performance, high speed, and low power dissipation may be difficult [2].

1.1 Types of Ram

i. Static RAM: SRAM may be a semiconductor memory style that uses bitable latching circuitry to store every bit. The term static RAM differentiates it from dynamic RAM that should be periodically refreshed. Static RAM exhibits data remanence; however, it's still volatile within the standard sense that knowledge is eventually lost once the memory isn't powered.

ii. Dynamic RAM: DRAM stores a small amount of data using a semiconductor device and capacitor combined with a Dynamic RAM cell. The condenser holds a high/low charge, and the semiconductor device acts as a switch that lets the control circuitry on the chip read the capacitor's state of charge or changes it. This memory manner is a smaller amount expensive to provide than static RAM; eventually, it's the predominant type of memory device utilised in modern computers. Dynamic RAM is volatile because it is lost |the information or data once power is off from the system [3].

1.2 Design of SRAM

A typical SRAM cell is created from six MOSFETs. Every bit in an SRAM is held on four transistors (M1, M2, M3, and M4) that kind two cross-coupled inverters. This secondary cell has 2 stable states that are wont to denote zero and one. two extra access transistors serve to manage the access to a secondary cell throughout reading and write operations. Additionally, to such six-transistor (6T) SRAM, different SRAM chips use four, 8, 10 (4T, 8T, 10T SRAM), or many transistors per bit. Four-transistor SRAM is sort of common in complete SRAM devices (as critical SRAM used for CPU caches), implemented in special processes with an additional layer of polysilicon, allowing for very high-resistance pull-up resistors. The principal disadvantage of using 4T SRAM is increased static power because of the constant current flow through all the pull-down transistors. Access to the cell is enabled by the word line that controls the two access transistors M5 and M6, which control whether the cell should be connected to the bit lines: BL and complementary BL. They're wont to transfer data for each scan and write operations. Though it's not strictly necessary to possess two-bit lines, each signal and its inverse are usually provided to enhance noise margins. The bit lines are actively driven high and low by the inverters within the SRAM cell throughout reading accesses. SRAMs' symmetric structure also permits differential signalling, making little voltage swings a lot simply detectable [4].

1.3 SRAM Memory Cell Operation

AN SRAM cell has three completely different states

i. Standby (the circuit is idle)

ii. Reading (the data has been requested)

iii. Writing (updating the contents)

i**. Standby**: If the word line isn't declared, the access transistors M5 and M6 disconnect the cell from the bit lines. The 2 cross-coupled inverters shaped by M1 – M4 can still reinforce one another as long as they're connected to the supply [5].

ii. Reading: In theory, reading only needs asserting the word line WL and reading the SRAM cell state by one access semiconductor and the bit line, e.g., M6, BL. However, bit lines are comparatively long and have massive parasitic capacitance. To speed up reading, an additional advanced method is used in practice: The browse cycle is started by recharging each bit lines BL and BL, i.e., driving the bit lines to a threshold voltage (midrange voltage between logical one and 0) by an external module (not shown within the figures). Then asserting the word line WL permits each the access transistors M5 and M6, which causes the bit line BL voltage to either slightly drops m3 is ON, and high PMOS transistor M4 is off) or rise (top PMOS transistor M4 is on). It ought to be noted that if BL voltage rises, the BL voltage drops, and vice versa. Then the BL and BL lines can have little voltage distinction between them. A way amplifier can sense that line has the upper voltage and therefore verify whether or not there was 1 or 0 stored. The upper the sensitivity of the sense amplifier, the quicker the browse operation [6].

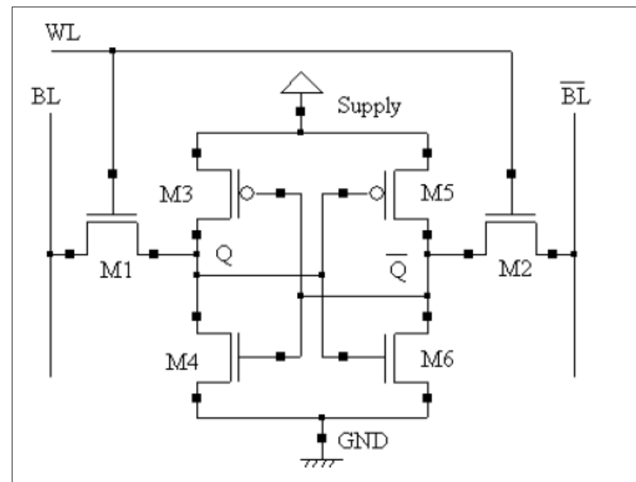

Fig 1 Design approach of SRAM

iii. Writing: The writing cycle begins by applying the value to the bit lines. If we would like to write a zero, we'd apply a zero to the bit lines, i.e., setting BL to one and BL to zero. This is often like applying a reset pulse to an SR-latch that causes the flip flop to alter state. A one is written by inverting the values of the bit lines. WL is then declared, and therefore the value that's to keep is secured.

This works as a result of the bit line input-drivers are designed to be much stronger than the relatively weak transistors within the cell itself to override the previous state of the cross-coupled inverters simply. In follow, access NMOS transistors M5 and M6 have to be compelled to be stronger than either bottom NMOS (M1, M3) or high PMOS (M2, M4) transistors. This is often obtained as PMOS transistors are much weaker than NMOS once same sized. Consequently, once one semiconductor combines (e.g., m3 and M4) is only slightly overridden by the write method, the other transistors combine (M1 and M2), a gate voltage is additionally modified. This means that the M1 and M2transistors are often easier overridden, and so on. Thus, cross-coupled inverters amplify the writing method [7-8].

II.LITERATURE SURVEY

Liu J et al. [9]. Proposes 6T. Fig. 2 shows the circuit diagram of a conventional SRAM cell. Before the read operation begins, the bit line (BL) and bitbar line (BLB) are precharged to as high as supply voltage vdd. When the word line (WL) is selected, the access transistors are turned on. This will cause a current to flow from the supply voltage (Vdd) through the pull-up transistor TP1 of the node storing "1". The current will flow from the precharged bit bar line to the ground, thus discharging a bit bar line. Thus, a differential voltage develops between the BL and BL. This small potential difference between the bit lines is sensed and amplified by the sense amplifiers at the data output.

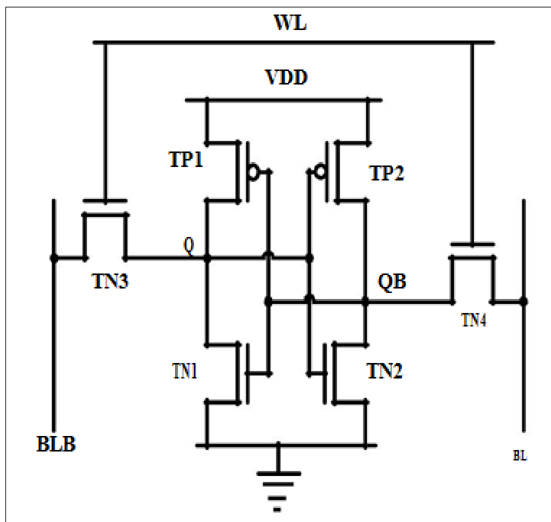

Fig2 Design 6T SRAM

Shilpi Birla1 et al. [10]. Analysed 8T Static Random Access Memory cell at 65nm process technology is shown in fig.3 This topology was originally proposed for a subthreshold static RAM design and optimised for functionality and performance over a large voltage range. A write operation is performed through WWL, WBL and WBLX port, whereas single-ended read operation is exercised through RWL and RBL ports. RBL is precharged at the end of each read cycle and keeps precharged during a write cycle. In this bit, cell write and read ports are decoupled compared to the traditional 6T cell. Read-SNM problem is eliminated, and 6T static RAM part can be sized for better writability without trading off RSNM. This makes the voltage drop across un-accessed read buffers zero, and hence leakage on the read bit line is highly reduced. Vdd is the virtual supply nodes for the cross-coupled inverters, and its voltage can be brought down during write access to weaken the PMOS load device and ease the write ability problem at low voltage**e**. Since the entire bit cells on a row are written and read simultaneously, Vdd is shared across one memory cell row.

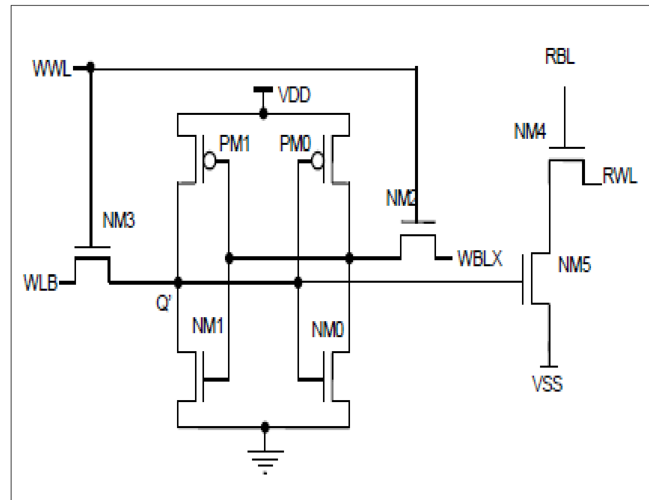

Fig3 8T SRAM cell

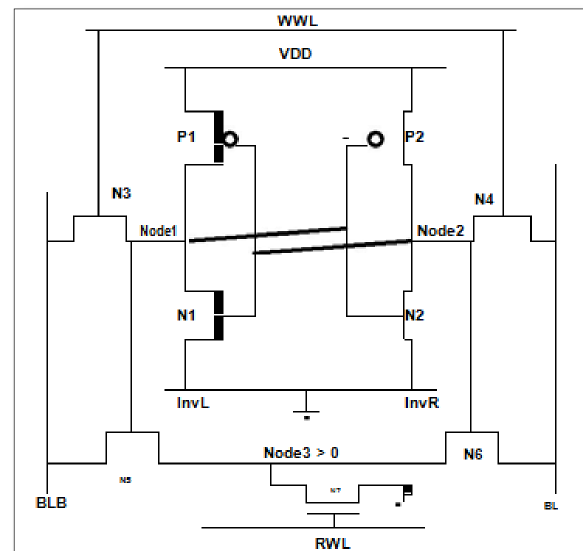

Fig4 9T SRAM Cell

Kursun V. et al. [11]. Introduce 9T SRAM is shown in Fig.4. Write occurs just as in the 6T SRAM cell. Reading occurs separately through N5, N6 and N7 controlled by the read signal (RWL) going high. This design has a high bit line

capacitance problem with more pass transistors on the bit line.

III. PROBLEM DECLARATION

Computer memories used to storage large data in this field, but every device needs power backup .main problem more power dissipation in Static random access memory cell structure. It is a most demandable unit of portable devices like PC, mobile phone and hard disk. The previous dissertation on 6T and 9T the leakage problem at the cost of degradation in another parameter like read access time, write access time and layout area for 6T,8T and 9T. This paper aims to reduce power dissipation during the Write operation in the CMOS SRAM cell. Another factor like- cell area, switching delay, power dissipation, and how many transistors are used in implementing SRAM are also optimising.

IV. SIMULATION TOOLS

The micro wind software system permits the designer to simulate and style a computer circuit at the physical description level. Born in Toulouse (France), the micro wind is an innovative CMOS style tool for the academic market. Pave their path for additional skilful software to be used at a later stage of their course work. Microwind is developed as a comprehensive package on the Windows platform to change students' sensible style strategies and additional observation techniques. With intrinsic layout writing tools, mix-signal machine, MOS characteristic viewer and additional, it permits students to find out complete style method with ease. Micro wind tool unifies schematic and pattern-based mostly machine also SPICE extraction of schematic using layout compilation, layout mix-signal circuit simulation, cross-sectional & 3D viewer, web list extraction, BSIM4 tutorial on MOS devices and sign-off correlation to deliver unmatched style performance and productivity. With its approach for CMOS style education, the small wind has gained heap followers worldwide. Universities across the world are victimisation micro wind for budding engineers to show CMOS ideas with ease. Pave their path for additional skilful software to be used at the later stage of their course work—the tool options full writing facilities, varied views, and an on-line analog machine. The Micro wind software system permits the designer to simulate and style a computer circuit at the physical description level.

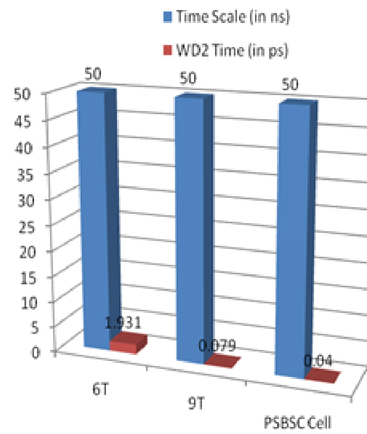

Figure 5 Compare WD Time analysis between 6T, 9T and PSBSC Cell

V. RESULT ANALYSIS

Proposed design circuit Proposed Static Random-Access Memory based on switching concept (PSBSC) Cell be extracted. Presented circuit 6T SRAM cell and 9T SRAM cell compare to our proposed design circuit proposed static random-access memory based on switching concept (PSBSC) Cell get Low-Power consumption.

(a) Proposed PSBSC circuit writes delay minimises and presented the circuit more write delay.

(b) Proposed PSBSC circuit read delay minimise and presented the circuit with more read delay.

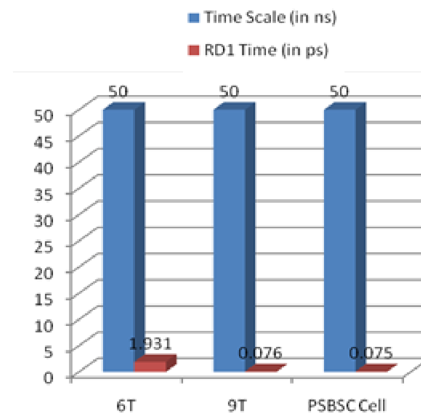

Figure 6. Compare RD Time analysis between 6T, 9T and PSBSC Cell

(c) Proposed PSBSC circuit power consumption minimises and presented the circuit with more power consumption.

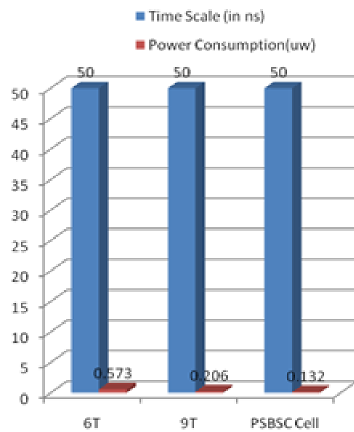

Figure 7. Compare Power Consumption Analysis between 6T, 9T and PSBSC Cell

VI.CONCLUSION

Enhancement performance static random access memory cell using a switching concept. An intensive survey has been finished on the various design of Static Random-Access Memory. Proposed static random-access memory (PSBSC) supported switching concept designs are well preferred for various low power applications and reduce the facility dissipation. It is often used for low power and high-speed applications. Design low power dissipation SRAM, low switching delay and fewer area optimisations. It's a basic structure block of the CPU of a computer. SRAM may be a structure block of several circuits. Understanding how an SRAM is designed and its works are important to putting together any advanced logic circuits design. Circuits design consists of various quite logic invertors, NMOS and flip-flop. Simply, to work on bit SRAMs. The micro wind program allows the designer to style and simulate a microcircuit at the physical description level. PSBSC cell is meant for top speed operation, with low power technique using small voltage swings on the bit-lines during the write operation. The 10T with switching format exhibited enormous read stability compared to the basic SRAM format. Also, it had been found that the foremost stable type of PSBSC cell is often designed by keeping the cell ratio as minimum as the unit of power.

Basic SRAM standby leakage power dissipation more and also the cell was expected at similar sizing of the transistors. It's almost capable of basic SRAM write delay and 9T. The 9T SRAM structure uses basic SRAM, and the 9T SRAM benefits using the 2-bit lines and even various read and write lines. The existing circuit basic SRAM cell and 9T SRAM cell compare to our proposed design circuit. PSBSC Cell gets Low-Power consumption. The proposed static random-access memory (PSBSC) designed an effective SRAM circuit and enhanced SRAM cell performance results based on low power consumption. The proposed static random-access memory (PSBSC) cell consumes very less power and has less read and write time. Higher cell ratios can decrease the read and write time, improve stability, be very effective, and simulate a micro wind tool.

REFERENCE

[1]. Jain, S. K., and Agarwal, P., "A Low Leakage and SNM Free SRAM Cell Design in Deep Submicron CMOS Technology", 19th International Conference on VLSI Design, Hyderabad, India, pp. 495-498, 2006.
[2]. Asenov, A., Brown, A. R., Davies, J. H., Kaya, S., and Slavcheva, G. "Simulation of Intrinsic Parameter Fluctuations in Decananometer and Nanometre-scale MOSFETs", IEEE Transactions on Electron Devices, vol. 50, No. 9, pp. 1837-1852, 2003.
[3]. Anurag Dandotiya and Amit S. Rajput," SNM Analysis of 6T SRAM at 32NM and 45NM Technique," IJCA, vol.98, no.7, July 2014.
[4]. Rupesh Maheshwari, Yogeshver Khandagre, Alok Dubey, "A Survey of Design Technology for SRAM", International Journal of Emerging Technology and Advanced Engineering, (ISSN 2250-2459, ISO 9001:2008 Certified Journal, Volume 3, Issue 11, November 2013.
[5]. Naveen Verma," Ultra-Low-Power SRAM Design in High Variability Advanced CMOS," May 2009.
[6]. Sanjeev K. Jain and Pankaj Agarwal "A Low Leakage and SNM Free SRAM Cell Design in Deep Submicron CMOS Technology "Proceedings of the 19th International Conference VLSI Design (VLSID'06), 2006.
[7]. Shigeki Ohbayashi, Makoto Yabuuchi, Koji Niiand, Susumu Imaoka "A 65-nm SoC Embedded 6T-SRAM Designed for Manufacturability with Reading and Write Operation Stabilizing Circuits" IEEE journal of solid-state circuits, Vol. 42, pp820 -829, April 2007.
[8]. Rajasekhar Keerthi and Chein-in Henry Chen "Stability and Static Noise Margin Analysis of Low-Power SRAM" I2MTC 2008 – IEEE International Instrumentation Measurement Technology Conference, Victoria, Vancouver Island, Canada, May 12-15, 2008.
[9]. Kim TH, Liu J, Keane J, Kim CH. Circuit techniques for ultra-low power sub-threshold SRAMs. IEEE international symposium on circuits and systems (ISCAS), p. 2574–77, 2008.
[10]. Shilpi Birla1, Neeraj Kumar Shukla, Kapil Rathi, Rakesh Kumar Singh, Manisha Pattanaik," Analysis of 8T SRAM Cell at Various Process Corners at 65 nm Process Technology," Circuits and Systems, pp.326-329, 2011.
[11]. Liu Z, Kursun V. Characterization of a novel nine-transistor SRAM cell. IEEE Trans Very Large Scale Integr (VLSI) Syst, 16:488–92. No. 4, 2008.
[12]. E. Grossar, M. Stucchi, K. Maex and W. Dehaene, "Read Stability and Write-Ability Analysis of SRAM Cells for Nanometre Technologies," IEEE J. Solid-State Circuits, Vol. 41, no. 11, pp. 2577-2588, Nov. 2006.

[13]. A. Rajendran, Y. Shiyanovskii, F. Wolff and C. Papachristou, "Noise Margin, Critical Charge and Power-Delay Trade-offs for SRAM Design," in 2011 IEEE 17th Int. On-Line Testing Symp., Jul. 2011, pp. 145-150.
[14]. M. Anis and M. H. Aburahma, "Leakage Current Variability in Nanometre Technologies," in 2005 Proc. 5th Int. Workshop on System on- Chip for Real-Time Application., Jul. 2005, pp. 60-63.
[15]. R.R. Rao, A. Devgan, D. Blaauw and D. Sylvester, "Parametric Yield Estimation Considering Leakage Variability," in 2004 Proc. 41st Design Automation Conf., Jul. 2004, pp. 442-447.
[16]. B. H. Calhoun and A. P. Chandrakasan, "Static Noise Margin Variation for Sub-threshold SRAM in 65-nm CMOS," IEEE J. Solid-State Circuits, Vol. 41, no. 7, pp. 1673-1679, Jul. 2006.
[17]. G. Razavipour, A. Afzali-Kusha and M. Pedram, "Design and Analysis of Two Low-Power SRAM Cell Structures," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., Vol. 17, no. 10, pp. 1551-1555, Mar. 2009.